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Patent
Attorney's Docket No. 032219-020

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

UTILITY PATENT
APPLICATION TRANSMITTAL LETTER

Box PATENT APPLICATION
Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Enclosed for filing is the utility patent application of Brian Sander and Earl W. McCune, Jr. for PLL NOISE SMOOTHING USING DUAL-MODULUS INTERLEAVING.

Also enclosed are:

[X] 6 sheet(s) of [ ] formal [X] informal drawing(s);

[ ] a claim for foreign priority under 35 U.S.C. §§ 119 and/or 365 is [ ] hereby made to _ filed in _ on ___;
[ ] in the declaration;

[ ] a certified copy of the priority document;

[ ] a Constructive Petition for Extensions of Time;

[ ] ______ statement(s) claiming small entity status;

[ ] an Assignment document;

[ ] an Information Disclosure Statement; and

[X] Other: a return postcard.

The unexecuted declaration of the inventor(s) [X] also is enclosed [] will follow.

[ ] Please amend the specification by inserting before the first line the sentence --This application claims priority under 35 U.S.C. §§119 and/or 365 to _ filed in _ on _; the entire content of which is hereby incorporated by reference.--

The filing fee has been calculated as follows [ ] and in accordance with the enclosed preliminary amendment:

CLAIMS					
	NO. OF CLAIMS		**EXTRA CLAIMS**	**RATE**	**FEE**
Basic Application Fee					$760.00
Total Claims	8	MINUS 20 =	0	x $18.00	0
Independent Claims	6	MINUS 3 =	3	x $78.00	234.00
If multiple dependent claims are presented, add $260.00					0
Total Application Fee					994.00
If verified Statement claiming small entity status is enclosed, subtract 50% of Total Application Fee					0
Add Assignment Recording Fee of $40.00 if Assignment document is enclosed					0
TOTAL APPLICATION FEE DUE [FEE NOT INCLUDED]					**$994.00**

Please address all correspondence concerning the present application to:

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Respectfully submitted,

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PLL NOISE SMOOTHING USING DUAL-MODULUS INTERLEAVING

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to phase locked loops (PLLs).

2. State of the Art

Practically all modern signal generators and radio communications equipment make widespread use of PLLs. A known PLL is shown in Figure 1. A reference frequency f_{in} is applied to a phase or phase/frequency detector, to which is also applied a feedback signal derived from an output frequency signal f_{out} of the PLL. The detector produces an error signal, which is filtered by a loop filter. An output signal of the loop filter is applied to a voltage-controlled oscillator (VCO), which produces the output frequency signal f_{out}. Commonly, a programmable divide-by-N counter divides down the output frequency signal f_{out} to produce a lower frequency signal that is then applied to the detector. In this manner, an output frequency signal can be generated that is some multiple of the reference frequency. Such divide-by-N counters are typically realized in CMOS.

At very high frequencies (such as those used in cellular radiotelephones), however, the speed capability of even the fastest CMOS circuit is quickly exceeded. In this instance, a dual-modulus prescaler is commonly used in which the difference between one divide modulus (P) and the other divide modulus (P + 1) is one. In such an arrangement, shown in Figure 2, a high-speed (e.g., ECL) dual-modulus counter is followed by a lower-speed (e.g., CMOS) programmable counter. The lower-speed counter controls which modulus of the dual-modulus prescaler is active at a given time via a modulus control signal MC. The use of multiple moduli enables a full range of effective divisors to be obtained.

One construction of such a circuit is shown in Figure 3, in which the dual-modulus counter is followed by a pair of lower-speed (e.g., CMOS) programmable counters. In the circuit of Figure 3, the reference and output frequencies are related

as follows:

$$
\begin{aligned}
f_{out} &= N \cdot f_{in} \\
&= (QP + R)f_{in} \\
&= ((Q - R)P + R(P + 1))f_{in}
\end{aligned}
$$

where Q is the quotient of the integer division N/P and R is the remainder of the integer division N/P. The value Q is used to preset a "tens" counter (so-called because its effect is multiplied by the modulus P) and R is used to preset a "ones" counter (the effect of which is not multiplied by the modulus). The value Q must be greater than or equal to the value R. With this restriction, the minimum division ratio achievable to guarantee continuous coverage of the possible integer divisors N using such a circuit is, in general, P(P - 1).

Assume, for example, that a 10/11 dual-modulus prescaler (P = 10) is used and that a desired output frequency is 197 times the reference frequency. Using the foregoing formula, Q might be 19 and R might be 7. (Note that R < P always.) These values are preset into the respective counters. With a non-zero value loaded into the R counter, the dual-modulus prescaler is set to divide by P + 1 at the start of the cycle. (The period of the cycle is given by the reciprocal of the reference frequency.) The output from the dual-modulus prescaler clocks both counters. When the R counter reaches zero, it ceases counting and sets the dual-modulus prescaler to divide by P. Only the Q counter is then clocked. Such a cycle is illustrated in Figure 4. When the Q counter reaches zero, the initial values are again loaded into the counters and the next cycle begins.

In such a circuit, the modulus control signal for controlling the dual-modulus prescaler can generate considerable noise within the frequency band of the reference signal, since the period of this modulus control signal is equal to the period of the PLL reference signal. Various filtering strategies have been used to attack

this problem. An effective, low-cost solution to this problem remains a long-standing need.

SUMMARY OF THE INVENTION

The present invention, generally speaking, achieves noise spreading within a PLL using a dual-modulus prescaler by interleaving the division moduli. Within a given cycle, "ones" and "tens" are not all counted consecutively. Instead, ones and tens are interleaved. In one embodiment of the invention, the R count is doubled and the output of the R counter is toggled between high and low states. (The Q counter may remain unmodified.) In another embodiment of the invention, ones and tens are interleaved in accordance with a ratio q:r. By so interleaving the modulus, the effect is to spread the noise resulting from the output signal of the dual-modulus prescaler over a wider frequency range. The prescaler noise level is greatly reduced, particularly within the frequency band of the reference frequency.

BRIEF DESCRIPTION OF THE DRAWING

The present invention may be further understood from the following description in conjunction with the appended drawing. In the drawing:

Figure 1 is a block diagram of a conventional PLL using a divide-by-N counter;

Figure 2 is a block diagram of a conventional PLL using a dual-modulus prescaler;

Figure 3 is a more detailed block diagram of one realization of the circuit of Figure 2;

Figure 4 is a timing diagram illustrating operation of the PLL of Figure 2;

Figure 5 is a diagram illustrating the principle of the invention in accordance with one embodiment thereof;

Figure 6 is a block diagram of a PLL in accordance with one aspect of the present invention;

Figure 7 is a timing diagram illustrating operation of the PLL of Figure 6;

Figure 8 is a waveform display showing noise levels using a conventional

PLL circuit; and

Figure 9 is a waveform display showing noise levels using the present PLL circuit.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The modulus interleaving technique of the present invention may be applied in various forms with varying degrees of sophistication and complexity. A simple but effective implementation of modulus interleaving is illustrated in Figure 5. In this implementation, the Q count and the Q counter are left unchanged. The R count is doubled, and the R counter is toggled. For example, if the R count would normally be 15 with the counter output being held low for 15 counts, instead the count is doubled to 30. The counter output, instead of being held low continuously, is toggled, i.e., low for 1 count, high for 1 count, low for 1 count, etc. The overall effect is the same as in the conventional case--referring again to the foregoing equations, the effect is to replace R with 2R/2. The difference is that the energy spectrum of the modulus control signal is shifted above and away from the PLL reference frequency. If desired, the same measure may be taken with respect to Q. In general, R (and Q, if desired) may be replaced by mR/m, where m is the number of moduli of the prescaler. For a dual modulus prescaler, m = 2.

In other arrangements, it may be advantageous to be able to control the distribution of pulses within the modulus control signal. Referring now to Figure 6, a block diagram is shown of a PLL circuit in accordance with another embodiment of the present invention. As compared to the PLL circuit of Figure 2, the R counter and the Q counter are modified by the addition of an r counter and an q counter, respectively. The resulting R counter counts R total counts, r at a time. The resulting Q counter counts Q total counts, q at a time. In accordance with an exemplary embodiment, the apparatus operates in the following manner.

As in the prior art circuit, with a non-zero value loaded into the R counter, the dual-modulus prescaler is set to divide by P + 1 at the start of the cycle. The

output from the dual-modulus prescaler clocks both counters. When the r counter reaches zero, the R counter ceases counting and sets the dual-modulus prescaler to divide by P. Only the Q counter is then clocked. When the q counter reaches zero, the initial values r and q are again loaded into the counters and the next subcycle begins. During the final subcycle, the R counter counts down to zero, after which the Q counter counts down to zero. Such operation is illustrated in Figure 7, with $(R, r) = (7, 1)$ and $(Q, q) = (8, 1)$. Note that r and q need not be one; the only requirements are that $R \leq Q$, $r \leq R$, and $q \leq Q$. (The case $r = R$ and $q = Q$ represents the conventional operating method.)

The noise spreading effect of the present modulus interleaving technique may be observed by comparing Figure 8 and Figure 9. Figure 8 is a plot of the energy within the signal present on the modulus control line in accordance with the traditional modulus control setup of Figures 3 and 4. Excluding zero hertz, the noise margin at the first noise peak is about -5dbm. Figure 9 is a plot of the energy within the signal present on the modulus control line in accordance with the present modulus control setup of Figures 6 and 7. Excluding zero hertz, the noise margin at the first noise peak is about -25dbm. Thus, this example demonstrates a reduction in the noise from the modulus control signal at the reference frequency of 20dB. Note that there are no additional components or extra filtering required by this method. There is essentially no increase in the cost of a PLL incorporating the present invention. Note further that this interleaving is readily expanded to higher order multi-modulus prescaling, such as 3-modulus and 4-modulus prescalers.

It will be appreciated by those of ordinary skill in the art that the invention can be embodied in other specific forms without departing from the spirit or essential character thereof. The presently disclosed embodiments are therefore considered in all respects to be illustrative and not restrictive. The scope of the invention is indicated by the appended claims rather than the foregoing description, and all changes which come within the meaning and range of equivalents thereof are intended to be embraced therein.

What is claimed is:

1. A method of operating a multiple-modulus prescaler having at least a modulus P and controlled by counting transitions of an applied frequency signal, comprising:

determining at least one of an integer portion Q and a remainder portion R of a division operation N/P, where a desired output frequency is N times an input reference frequency;

during at least a portion of a modulus control signal, alternating ~~the~~ modulus control signal between high and low states such that a maximum number of counts that the modulus control signal resides within a given state is less than R.

2. The method of Claim 1, further comprising toggling the modulus control signal between states at ~~each~~ count.

3. A multiple-modulus prescaler and associated control circuitry, operated by counting transitions of an applied frequency signal, comprising:

a first counter, including means for storing a first preset count, for counting transitions of the applied frequency signal; and

a second counter, including means for storing a second preset count, for counting transitions of the applied frequency signal;

wherein at least one of the counters, during counting of the preset count, generates an output signal that transitions multiple times.

4. A method of operating a multiple-modulus prescaler, comprising:

controlling selection between at least a first and second modulus on a cycle basis such that over the course of a cycle the prescaler divides an applied frequency signal by the first modulus for a first proportion of the

cycle and divides the applied frequency signal by the second modulus for a second proportion of the cycle; and

controlling selection between at least the first and second modulus on a subcycle basis such that over the course of a subcycle the prescaler divides the applied frequency signal by the first modulus for a first proportion of the subcycle and divides the applied frequency signal by the second modulus for a second proportion of the subcycle.

5. The method of Claim 4, wherein said cycle includes multiple subcycles.

6. A method of operating a phase locked loop that receives a reference frequency and produces a output frequency, the phase locked loop including a multiple-modulus prescaler, the method comprising the steps of:

determining for a desired output frequency a first proportion of a period, defined by the reciprocal of the input frequency, during which a first modulus is to be used, and determining a second proportion of the period during which a second modulus is to be used; and

controlling the modulus so as to change modulus a multiplicity of times during a period so as to obtain the desired output frequency.

7. A control circuit for a multiple-modulus prescaler, comprising:

a first counter that counts R total counts r at a time;

a second counter that counts Q total counts q at a time; and

a control circuit for repeatedly selecting in turn a first modulus for r counts and a second modulus for q counts.

8. A phase locked loop comprising:

a reference frequency signal;

a detector coupled to the reference frequency signal;

a loop filter coupled to an output signal of the detector;

a controlled oscillator coupled to an output signal of the loop filter, the controlled oscillator producing an output frequency signal; and

a frequency division circuit responsive to the output frequency signal for producing a feedback signal that is applied to the detector, the frequency division circuit comprising:

a multiple-modulus prescaler;

a first counter that counts R total counts r at a time;

a second counter that counts Q total counts q at a time; and

a control circuit for repeatedly selecting in turn a first modulus for r counts and a second modulus for q counts.

ABSTRACT OF THE DISCLOSURE

The present invention, generally speaking, achieves noise spreading within a PLL using a dual-modulus prescaler by interleaving the division moduli. Within a given cycle, "ones" and "tens" are not all counted consecutively. Instead, ones and tens are interleaved. In one embodiment of the invention, the R count is doubled and the output of the R counter is toggled between high and low states. (The Q counter may remain unmodified.) In another embodiment of the invention, ones and tens are interleaved in accordance with a ratio q:r. By so interleaving the modulus, the effect is to spread the noise resulting from the output signal of the dual-modulus prescaler over a wider frequency range. The prescaler noise level is greatly reduced, particularly within the frequency band of the reference frequency.

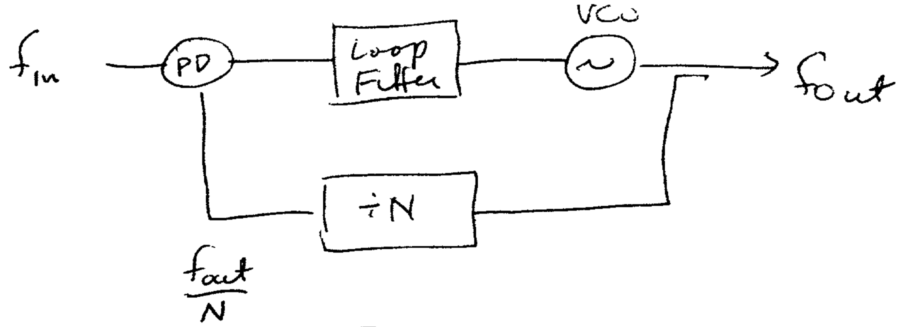

FIG 1
(PRIOR ART)

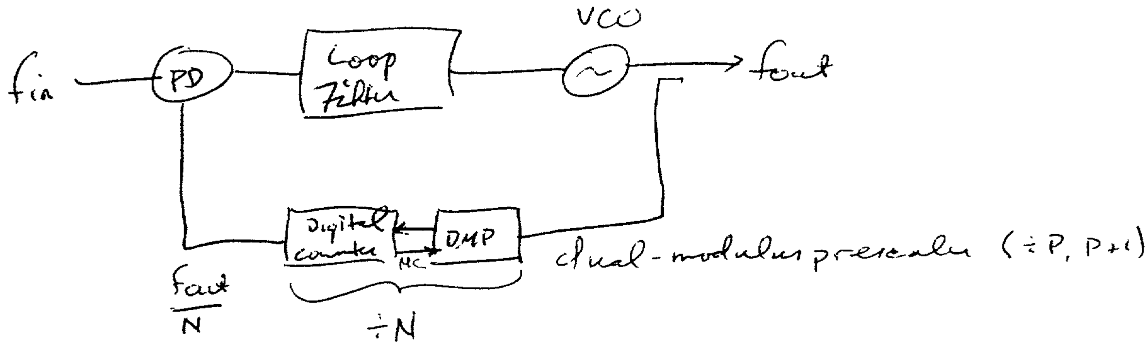

FIG 2
(PRIOR ART)

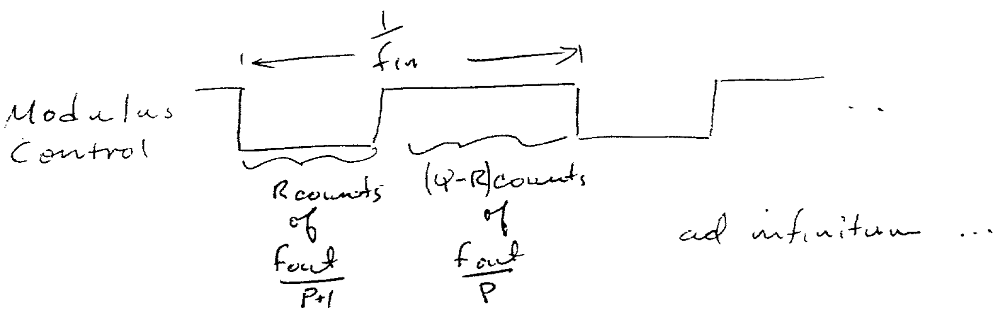

FIG 4
prior art

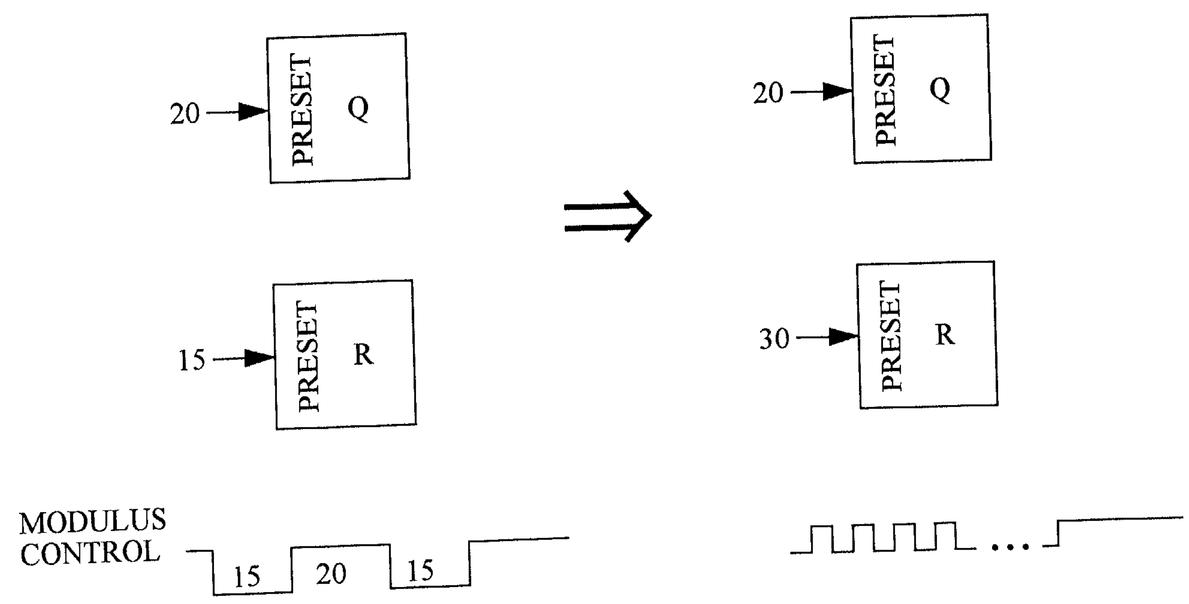
20
PRESET
Q
15
PRESET
R
20
PRESET
Q
30
PRESET
R
MODULUS
CONTROL
15
20
15

Fig. 5

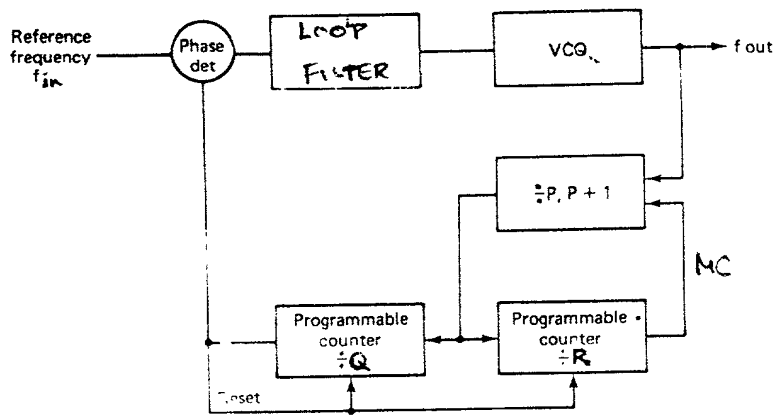

FIG 3
(PRIOR ART)

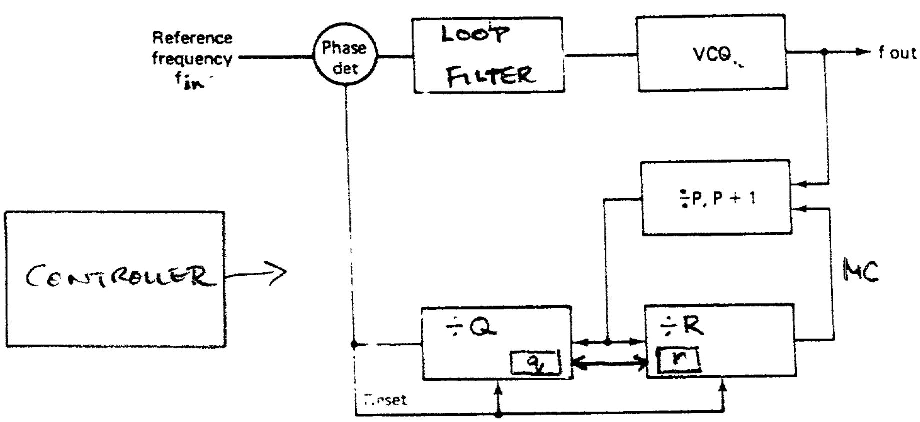

FIG 6

Example: $R = 7$ $Q = 15$
$(Q-R = 8)$

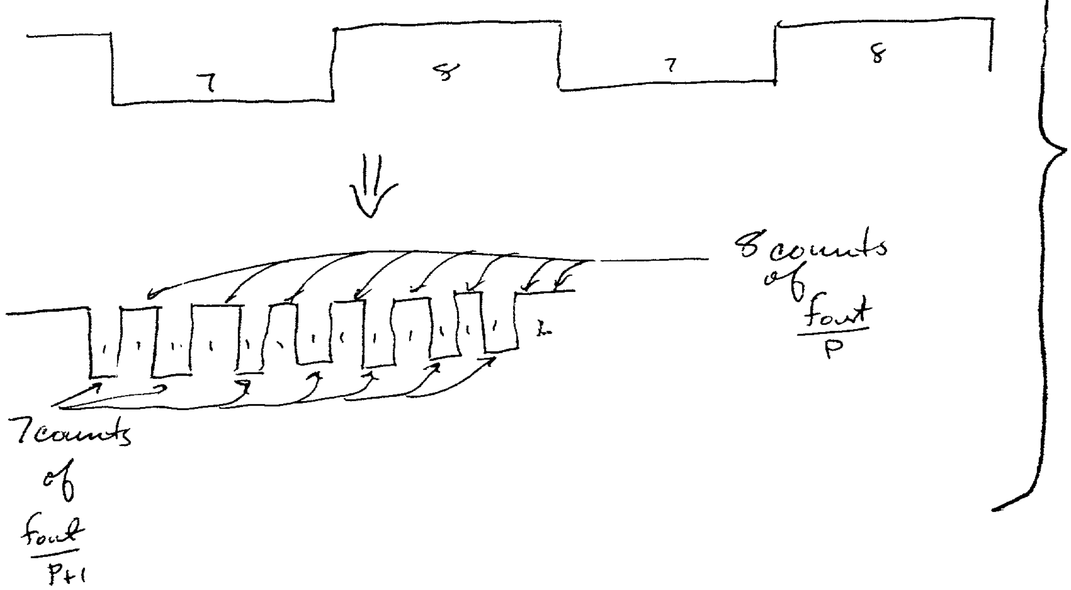

FIG 7

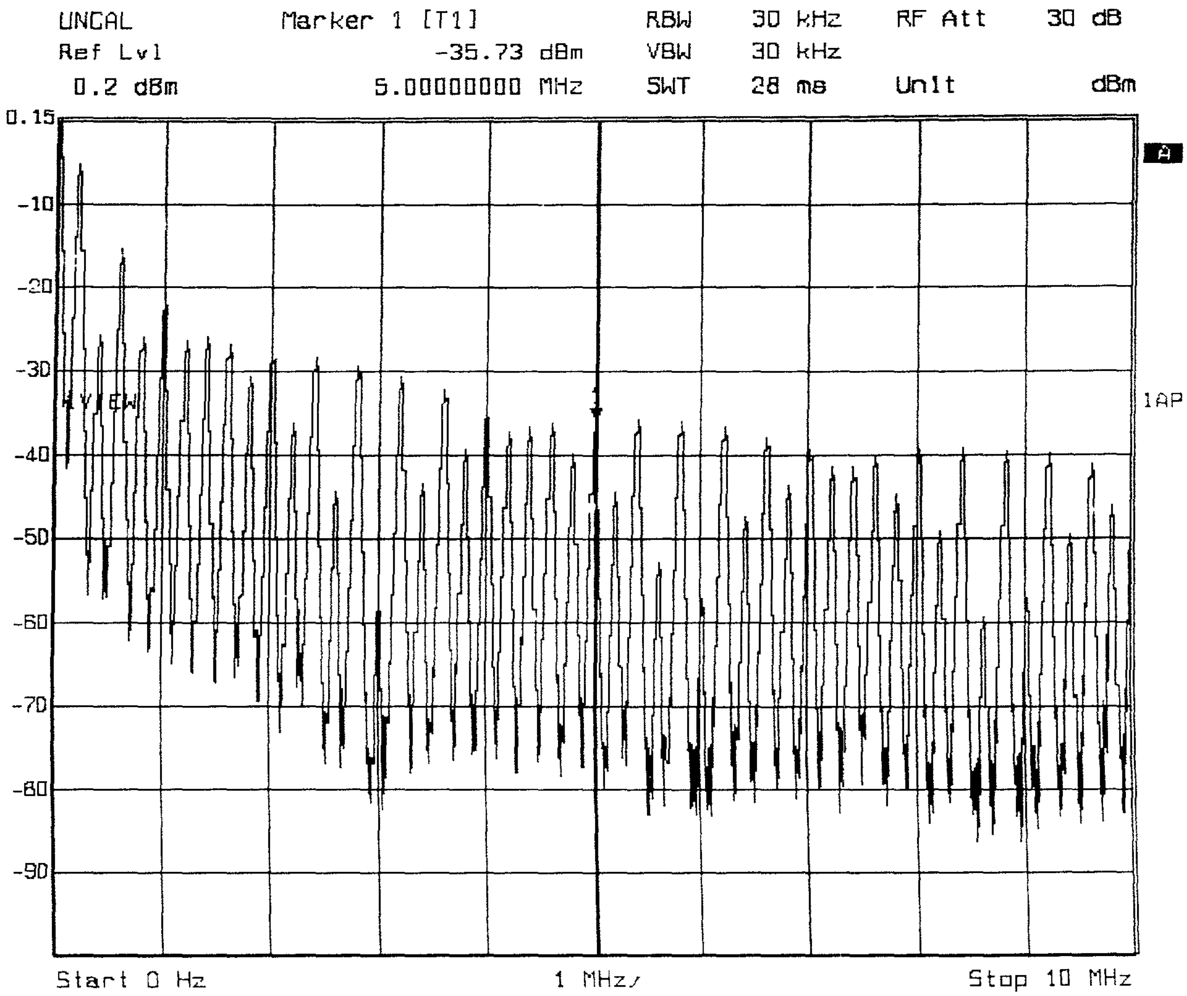

FIG 8
(PRIOR ART)

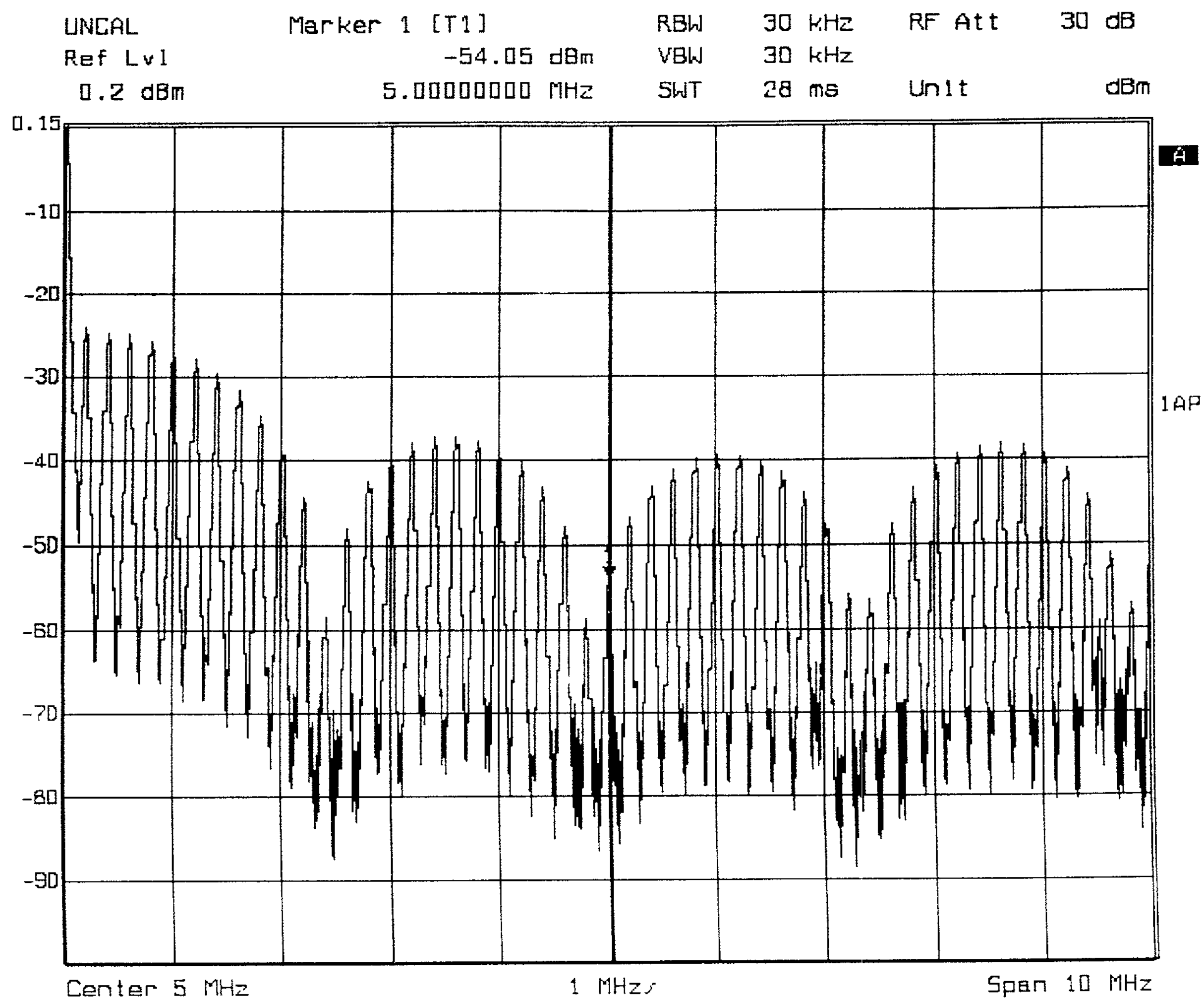
UNCAL
Marker 1 [T1]
RBW 30 kHz
RF Att 30 dB
Ref Lvl
-54.05 dBm
VBW 30 kHz
0.2 dBm
5.00000000 MHz
SWT 28 ms
Unit dBm
0.15
-10
-20
-30
-40
-50
-60
-70
-80
-90
A
1AP
Center 5 MHz
1 MHz/
Span 10 MHz

FIG 9

COMBINED DECLARATION AND POWER OF ATTORNEY FOR UTILITY PATENT APPLICATION	Attorney's Docket No. 032219-020

As a below-named inventor, I hereby declare that:
My residence, post office address and citizenship are as stated below next to my name;
I BELIEVE I AM THE ORIGINAL, FIRST AND SOLE INVENTOR (if only one name is listed below) OR AN ORIGINAL, FIRST AND JOINT INVENTOR (if more than one name is listed below) OF THE SUBJECT MATTER WHICH IS CLAIMED AND FOR WHICH A PATENT IS SOUGHT ON THE INVENTION ENTITLED:

PLL NOISE SMOOTHING USING DUAL-MODULUS INTERLEAVING

the specification of which

(check one) [X] is attached hereto;
[ ] was filed on ______________ as
Application No. ______________
and was amended on ______________;
(if applicable)

I HAVE REVIEWED AND UNDERSTAND THE CONTENTS OF THE ABOVE-IDENTIFIED SPECIFICATION, INCLUDING THE CLAIMS, AS AMENDED BY ANY AMENDMENT REFERRED TO ABOVE;

I ACKNOWLEDGE THE DUTY TO DISCLOSE TO THE OFFICE ALL INFORMATION KNOWN TO ME TO BE MATERIAL TO PATENTABILITY AS DEFINED IN TITLE 37, CODE OF FEDERAL REGULATIONS, Sec. 1.56 (as amended effective March 16, 1992);

I do not know and do not believe the said invention was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to said application; that said invention was not in public use or on sale in the United States of America more than one year prior to said application; that said invention has not been patented or made the subject of an inventor's certificate issued before the date of said application in any country foreign to the United States of America on any application filed by me or my legal representatives or assigns more than twelve months prior to said application;

I hereby claim foreign priority benefits under Title 35, United States Code Sec. 119 and/or Sec. 365 of any foreign application(s) for patent or inventor's certificate as indicated below and have also identified below any foreign application for patent or inventor's certificate on this invention having a filing date before that of the application(s) on which priority is claimed:

 (07/99)

COMBINED DECLARATION AND POWER OF ATTORNEY	Attorney's Docket No. 032219-020

COUNTRY/INTERNATIONAL	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED
			YES_ NO_
			YES_ NO_

I hereby appoint the following attorneys and agent(s) to prosecute said application and to transact all business in the Patent and Trademark Office connected therewith and to file, prosecute and to transact all business in connection with international applications directed to said invention:

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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